REMARKS

This is a full and timely response to the non-final Office action mailed May 31, 2006. Reexamination and reconsideration in view of the foregoing amendments and following remarks is respectfully solicited. Claims 1-18 are pending in this application, with Claims 1, 8 and 12 being the independent claims. Claims 1, 2, 5, 8 and 12 have been amended. No new matter is believed to have been added.

Claim Objections

Without consenting to the rejections set forth in the Office Action, we have amended the "first interface" and "second interface" language in claims 1-7 to refer to the two interfaces as a "target interface" and a "master interface", respectively. We have also made several merely linguistic changes to the claims (particularly claims 1 and 8) to clarify that these claims are not intended to be interpreted under 35 U.S.C § 112, paragraph 6, and to remedy other minor readability issues not pointed out by the Examiner. These changes are purely linguistic in nature, are not made for purposes relating to patentability, and therefore do not affect the scope of any legal equivalents that would otherwise be available. Reconsideration is requested.

Prior Art Rejections

Claims 1-5, 7-9, and 12 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,991,900 (Garnett). Claim 12 was rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 6,145,044 (Ogura). Various other claims were rejected under various Section 103 combinations of references. We respectfully traverse each of these rejections in that the cited references fail to anticipate our claimed inventions.

In highly safety-conscious environments (such as avionics), there is a significant need to protect the stability and integrity of the buses interconnecting various electronic components (e.g. flight management computers, air traffic warning systems, ground proximity warning, radio or radar systems, autopilot, and/or the like). As a result, various proprietary bus designs have been formulated to ensure very highly reliable communications between components. The cost of proprietary bus schemes, however, can be significant compared to the cost of commercial off-the-shelf (COTS) buses used in personal computing environments and the like. The present invention overcomes this shortcoming by providing a highly reliable bus architecture that is capable of using COTS I/Os without sacrificing reliability.

To improve the reliability of a COTS I/O, an isolator is provided between the I/O and the protected bus. The presence of the isolator allows two primary benefits: (1) the isolator can verify the integrity of the data before the data is sent on the protected bus; and (2) the isolator can contain a target interface that only allows data on the protected bus in response to an instruction from the bus controller. One example of this is described in our specification at, for example, paragraph 0026.

Unlike our claimed inventions, the primary reference cited in the Office Action, Garnett, simply describes a bus controller for use within a personal computer. The bus controller has a bridge (element 12 in FIG. 1) that allows data to be transmitted between separate processing buses (buses 24 and 26 in FIG. 1) and peripheral buses (the "D-BUS" in FIG. 1). This scheme is described in detail at the top of Garnett's column 4. Importantly, the Garnett system does not disclose any sort of integrity verification system, nor does it describe data being allowed on a protected bus only in response to a request from a bus controller. Both of these aspects are now effectively recited in each of our independent claims.

In the previous rejection of claim 2, the Office Action does allege that Garnett discloses at least some aspects whereby a defective I/O cannot capture the bus, citing to col. 12, lines 24-33 and col. 7, lines 48-55 of Garnett. From looking at the cited language, however, it is apparent that Garnett contemplated no such thing. The cited language from Column 12, for example, merely relates to conventional parity checking for virtual memory. Even if the stored data fails its parity check, there is no mention of any structure that limits access to the protected bus except as requested from a remote bus controller. The col. 7 language similarly fails to disclose these aspects of our claims. To the contrary, this language simply describes the function of "disconnect registers" (element 120 in FIG. 7) that store data for recovery following an error condition.

The Ogura reference is not alleged to disclose the various elements now found in claim 12, and therefore a detailed analysis of the reference need not be presented here. Nevertheless, we do point out that Ogura similarly describes a personal-computing type bus that does not incorporate the robustness features that are claimed within our independent claims. The other art of record is also not understood to disclose or suggest the inventive concept of the present invention as defined by the claims.

Because the various dependent claims add additional limitations to the independent

claims, the dependent claims are patentable *a fortiori*. A detailed analysis of the rejections of the dependent claims therefore would be cumulative. While we reserve the right to separately argue the patentability of any dependent claim at a later date, our analysis in this response primarily focuses on claims 1, 8 and 12 inasmuch as the other claims will be deemed patentable in view of the arguments presented above.

Based on the above, independent Claims 1, 8 and 12 are patentable over the citations of record. The dependent claims are also deemed patentable for the reasons given above with respect to the independent claims and because each recite features which are patentable in its own right. Individual consideration of the dependent claims is respectfully solicited.

Conclusion

We therefore submit that the present application is in condition for allowance. Favorable reconsideration and withdrawal of the objections and rejections set forth in the above-noted Office action, and an early Notice of Allowance are requested. If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone the undersigned attorney at the below-listed number. If for some reason Applicant has not paid a sufficient fee for this response, please consider this as authorization to charge Ingrassia, Fisher & Lorenz, Deposit Account No. 50-2091 for any fee which may be due.

Respectfully submitted,

INGRASSIA FISHER & LORENZ

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By: _____

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